REMARKS

I. STATUS OF CLAIMS

In accordance with 37 C.F.R. § 1.173(c), the status of the claims are as follows:

Claims 1-33 and 40-56 are pending in the reissue application.

Claims 1-33 are original claims and remain allowed. No changes have been made to claims 1-33.

Claims 34-54 were previously added in the preliminary amendment filed November 24, 2003, with claims 34-39 being canceled in the amendment filed November 20, 2006.

Claims 40 and 47 are being amended in the enclosed amendment, and claims 55-56 are newly added.

No new matter has been added.

II. EXPLANATION OF SUPPORT IN DISCLOSURE FOR AMENDMENTS

Claim 40 has been amended as follows: "an execution unit which executes ~~capable of executing~~ up to N number of instructions ... wherein the decoding unit decodes ~~is capable of decoding~~ a plurality of instructions executed in parallel, and all of the instructions decoded in parallel at the same cycle pass through the bus." Claim 47 similarly has been amended as follows: "an execution unit that executes ~~capable of executing~~ ... and all of the instructions decoded in parallel at the same cycle pass through the bus." New claims 55-56 have been added. Support for the aforementioned features of the present invention can be found, for example, in Figures 4, 7 and 11 of Applicants' drawings and the corresponding disclosure in Applicants' specification.

III. CLAIM OBJECTION AND PRIOR ART REJECTION

Claim 40 stands objected to for a minor informality. It is respectfully submitted that the enclosed amendment obviates the alleged informality. Accordingly, it is respectfully requested that this objection be withdrawn.

Claims 40-54 stand rejected under 35 U.S.C. § 102 as being anticipated by Sato et al. '710 ("Sato"). Claims 40 and 47 are independent. This rejection is respectfully traversed for the following reasons.

Claim 40 recites in pertinent part, "wherein the total bit width of the instruction bus is shorter than M * N bits, wherein the decoding unit decodes a plurality of instructions executed in parallel, *and all of the instructions decoded in parallel at the same cycle pass through the bus*" (emphasis added). Claim 47 similarly recites in pertinent part, "a decoding unit that decodes a plurality of instructions executed in parallel ..., wherein the total bit width of the instruction bus is shorter than M * N bits, ... *and all of the instructions decoded in parallel at the same cycle pass through the bus*" (emphasis added).

In order to read Sato on the claimed invention, the Examiner broadly interprets the bus width of the bus formed between INSTRUCT LATCH 211 and FORMAT DECODER 221 as being 16 bits to be shorter than 16*4 = 64 bits (Figure 6 of Sato). In so doing, the Examiner has necessarily interpreted the decoder 221 as the ***entire*** decoder in of itself. However, in reality, element 221 is merely one part of a decoder made up of elements 221, 222, 223, 224, 231, 232, 233, 234 ***collectively***. When interpreted this way, Sato does not disclose "the total bit width of the instruction bus is shorter than M * N bits." The Examiner does not appear to recognize that the claims embody a decoding unit which decodes a plurality of instructions executed in parallel.

That is, in contrast to the claimed invention, the interpreted decoder 221 of Sato can only decode a single instruction, so that Sato does not disclose the combination of features recited in the pending claims. Nevertheless, the Examiner maintains the same rejection by arguing that in Sato, "the bus connection to each decoder is 'an instruction bus' since each decoder has a separate instruction latch ... [and] since Sato's bus width as being 16 bits, it is shorter than 16*4 = 64 bits" (page 3, last four lines of outstanding Office Action).

However, by relying on a single instruction bus corresponding to ***one*** of the alleged decoders 221-224 as the claimed "instruction bus," the Examiner has overlooked the limitation in claim 40 (similarly in claim 47) that the decoding unit decodes a ***plurality*** of instructions executed in parallel. That is, none of the alleged decoders 221-224 ***individually*** decode a plurality of instructions executed in parallel, but rather only "decode" serially a single instruction to be executed. Accordingly, even assuming *arguendo* that the Examiner's reliance on a single instruction for a respective decoder 221-224 as the claimed "instruction bus" is proper, then the individual decoder of Sato does not decode a ***plurality*** of instructions executed in parallel as also claimed; so that Sato does not disclose the claimed ***combination*** of features.

Nonetheless, to further clarify the distinction between the present invention and Sato, claims 40 and 47 both embody all of the instructions decoded in parallel at the same cycle pass through the bus. Support for this feature can be found, for example, in Figure 4 of Applicants' drawings. In contrast, none of the respective instruction buses connected to a corresponding decoder 221-224 of Sato have all of the instructions ***decoded in parallel at the same cycle*** pass therethrough (*see* Figure 6 of Sato). In other words, all of the instructions which are decoded in parallel at the same cycle do NOT pass through a single 16-bit bus shown in Figure 6 of Sato. In fact, Sato is specifically arranged to divide data originally being 64-bit into four 16-bit pieces.

Instead, all of the instructions which are decoded in parallel at the same cycle pass through the ***collective*** decoders 221-224 so that the total bit width of the instruction bus of Sato would be equal to M * N bits; i.e., 16 * 4 = 64 bits. Indeed, Sato is merely cumulative to the conventional decoder/bus configuration, and there is no suggestion or motivation outside of Applicants' specification to configure the total bit width of the instruction bus to being shorter than M * N bits.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Sato does not anticipate claims 40 and 47, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 40 and 47 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

III. CONCLUSION

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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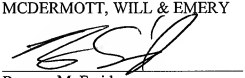

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